AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application.

Claims 1-11 (Cancelled).

12. (Currently Amended) A semiconductor device comprising a driver circuit for supplying a voltage at an output node in accordance with an input signal received at an input node, said driver circuit including:

a first transistor connected between a first voltage and the output node, and turned on and off in accordance with voltage level of a first internal node;

a second transistor connected between the output node and a second voltage, and turned on and off in accordance with voltage level of a second internal node;

a third transistor connected in parallel with said second transistor, between the output node and the second voltage, and turned on and off, complementarily to said first transistor, in accordance with the voltage level of the first internal node;

a control circuit for controlling voltages of the first and second internal nodes to complementarily turn on said first transistor and said second and third transistors in accordance with the input signal; and

a fourth transistor connected between the second voltage and the second internal node, wherein

said control circuit sets one of the first and second voltages for turning on said second and third transistors, turns off said first transistor when said second and third transistors are turned on, and supplies the one of the first and second voltages to the second internal node for a predetermined period, ~~and~~

said second transistor has a driving force for supplying the second voltage to the output node and higher than a driving force of said third transistor, and

said fourth transistor is turned on when said first transistor turns on.

13. (Previously Presented) The semiconductor device according to claim 12, wherein said control circuit includes a timing circuit connected to the second internal node and adjusting the predetermined period in accordance with the voltage level of the output node.

14. (Withdrawn) The semiconductor device according to claim 12, wherein said control circuit includes a connection circuit for electrically connecting the first internal node to the second internal node for the predetermined period.

15. (Withdrawn) The semiconductor device according to claim 12, wherein
the input signal includes a plurality of signals, and
said control circuit controls the voltages of the first and second internal nodes in accordance with a logic operation result, based on the plurality of signals.

16. (Previously Presented) The semiconductor device according to claim 12, wherein said first, second, third, and fourth transistors are field-effect transistors having respective gate oxide films, and said fourth field-effect transistor has a gate oxide film having a dielectric constant different from dielectric constant of said gate oxide film of at least one of said first, second, and third transistors.

17. (Withdrawn) The semiconductor device according to claim 13, wherein said timing circuit includes a noise adjustment circuit for supplying one of the first and second voltages for turning on said second and third transistors to the first internal node in response to an external instruction in a standby state.

Claim 18 (Cancelled).

19. (Previously Presented) The semiconductor device according to claim 12, wherein said timing circuit includes fifth and sixth transistors connected in series between the first voltage and the second internal node.

20. (Previously Presented) The semiconductor device according to claim 19, wherein said timing circuit includes an inverter, said fifth transistor has a control terminal connected to the input node, and said sixth transistor has a control terminal coupled to the output node through said inverter.

21. (Previously Presented) The semiconductor device according to claim 17, wherein
said timing circuit includes fifth and sixth transistors connected in series between the first voltage and the second internal node, and
said noise adjustment circuit comprises a seventh transistor connected in parallel with said sixth transistor and having a control terminal for receiving the external instruction.